Listing of Claims:

This listing of claims reflects all claim amendments and replaces all prior versions, and listings, of claims in the application (material to be inserted is in **bold and underline**, and material to be deleted is in ~~strikeout~~ or (if the deletion is of five or fewer consecutive characters or would be difficult to see) in double brackets [[ ]].

1. (Canceled)

2. (Canceled)

3. (Currently Amended) The phase-locked loop system of claim [[2]] **6**, where the plurality of outputs are configured to produce respective signals that are oriented at regular fixed phase relationships with the primary output signal.

4. (Original) The phase-locked loop system of claim 3, where the regular fixed phase relationships uniformly span 360 degrees.

5. (Original) The phase-locked loop system of claim 4, where the voltage-controlled oscillator includes four outputs and the regular fixed phase relationships are 0, -90, -180, -270 degrees.

6. (Currently Amended) **A phase-locked loop system, comprising:**

an error detector configured to receive a reference signal; and

a voltage-controlled oscillator subsystem coupled to the error detector, the voltage-controlled oscillator subsystem being configured to produce a primary output signal that tends toward a predefined frequency relationship with the reference signal, and to produce a feedback signal that is routed in a feedback loop back to the error detector,

where the voltage-controlled oscillator subsystem includes a multiple output voltage-controlled oscillator having a plurality of VCO outputs, each of the plurality of VCO outputs being configured to produce a phase-sifted signal based on the primary output signal, and

~~The phase-locked loop system of claim 2,~~ where the voltage-controlled oscillator subsystem further includes a VCO output multiplexer configured to multiplex the phase-shifted signals from the plurality of VCO outputs, to form the feedback signal.

7. (Original) The phase-locked loop system of claim 6, where the voltage-controlled oscillator subsystem further includes an incrementer coupled to the VCO output multiplexer, the incrementer being configured to produce an incrementer output value that drives the VCO output multiplexer.

8. (Original) The phase-locked loop system of claim 7, where the incrementer is clocked using the feedback signal output by the VCO output multiplexer.

9. (Original) The phase-locked loop system of claim 7, where the VCO output multiplexer is configured to select from among the plurality of VCO outputs based on the incrementer output value.

10. (Original) The phase-locked loop system of claim 9, where there are four VCO outputs and the incrementer output value is an integer selected from the group consisting of 0, 1, 2, and 3.

11. (Original) The phase-locked loop system of claim 7, where the incrementer output value is a number including an integer component, and the integer component is used to drive the VCO output multiplexer.

12. (Original) The phase-locked loop system of claim 7, where the incrementer is configured to receive incrementer input values from an input, and to produce the incrementer output values based on the incrementer input values.

13. (Original) The phase-locked loop system of claim 12, where the incrementer further includes an adder configured to sum incrementer input values over a period of time.

14. (Original) The phase-locked loop system of claim 7, where the incrementer is configured produce the incrementer output value based on an incrementer input value that varies over time according to a predetermined drift pattern.

15. (Original) The phase-locked loop system of claim 14, where the drift pattern is a sawtooth pattern.

16. (Original) The phase-locked loop system of claim 7, where the incrementer is configured to produce the incrementer output value based on an incrementer input value that includes a fractional component.

17. (Original) The phase-locked loop system of claim 16, where the fractional component of the incrementer input value causes the multiplexer to produce a feedback signal that does not have a constant cycle time.

18. (Original) The phase-locked loop system of claim 17, further comprising, a correcting charge pump coupled to the error detector, the correcting charge pump being configured to output correcting pulses in response to a detected phase error between the reference signal and the feedback signal.

19. (Original) The phase-locked loop system of claim 18, further comprising a filter network coupled to an output of the correcting charge pump, the filter network being configured to eliminate output ripple from the correcting charge pump.

20. (Original) The phase-locked loop system of claim 19, where the correcting charge pump and filter network are configured to provide both integrating and proportional control over the primary output signal.

21. (Original) The phase-locked loop system of claim 18, where the correcting charge pump is configured to output a correcting pulse having an undesirable portion resulting from an attempt by the correcting charge pump to compensate for the non-constant cycle time of the feedback signal.

22. (Original) The phase-locked loop system of claim 21, further comprising a canceling charge pump coupled to an output of the correcting charge pump, the canceling charge pump being configured to produce a canceling pulse to compensate for the undesirable portion of the correcting pulse.

23. (Original) The phase-locked loop system of claim 22, where the canceling pulse is opposite of the correcting pulse.

24. (Original) The phase-locked loop system of claim 22, where the canceling charge pump is configured to keep the pulse width of the canceling pulse constant and vary the amplitude of the canceling pulse.

25. (Original) The phase locked loop system of claim 22, where the canceling charge pump is coupled to a current source.

26. (Original) The phase-locked loop system of claim 25, where the current source is coupled to an output the incrementer, and is configured to be controlled by the fractional component of the incrementer output value.

27. (Original) The phase-locked loop system of claim 26, where the canceling charge pump and incrementer controlled current source are combined such that the charge pump switches are used to also select different current levels.

28. (Original) The phase-locked loop system of claim 26, where the canceling charge pump is configured to provide both integrating and proportional control over the primary output signal.

29. (Withdrawn) The phase-locked loop system of claim 22, where the correcting charge pump is one of a pair of correcting charge pumps coupled to the error detector, the pair of correcting charge pumps including a correcting integrating charge pump and a correcting proportional charge pump; and

where the canceling charge pump is one of a pair of canceling charge pumps, each of the canceling charge pumps being coupled to a respective output of one of the correcting charge pumps, the pair of canceling charge pumps including a canceling integrating charge pump and a canceling proportional charge pump.

30. (Original) The phase-locked loop system of claim 6, where the VCO output multiplexer is one of a pair of VCO output multiplexers coupled to the plurality of outputs of the voltage-controlled oscillator, a first VCO output multiplexer of the pair being configured to produce a feedback signal that is sent to the error detector, and a second VCO output multiplexer of the pair being configured to produce a leading or trailing feedback signal that is routed to the canceling charge pump via a second error detector.

31. (Original) The phase-locked loop system of claim 30, where the first and second error detectors are configured to adjust the timing of the correcting charge pump and the canceling charge pump, at least in part by keeping the canceling pulse of the canceling charge pump either leading or trailing the correcting pulse of the correcting charge pump.

32. (Original) The phase-locked loop system of claim 31, where the first and second error detectors are configured to adjust the timing of the correcting charge pump and the canceling charge pump, at least in part by keeping the canceling pulse of the canceling charge pump either beginning or ending at the same time as the correcting pulse of the correcting charge pump.

33. (Original) The phase-locked loop system of claim 6, where the voltage-controlled oscillator subsystem further includes an interpolator coupled to the multiplexer, the interpolator being configured to generate an output signal that is a phase-rotated version of the primary output signal, the interpolator output signal having a phase that is in between the predetermined fixed relationships of the VCO outputs.

34. (Original) The phase-locked loop system of claim 33, where the voltage-controlled oscillator subsystem further includes an incrementer coupled to the VCO output multiplexer, the incrementer being configured to produce an incrementer output value that drives the VCO output multiplexer, and where the incrementer is clocked using an output of the interpolator.

35. (Currently Amended) The phase-locked loop system of claim [[1]] **6**, further comprising a divider positioned intermediate the voltage-controlled oscillator subsystem and the error detector, the divider being configured to divide the feedback signal by a predetermined value before the feedback signal is sent to the error detector.

36. (Original) The phase-locked loop system of claim 35, where the divider output is used as an enable for the reference signal input of the error detector.

37. (Currently Amended) The phase-locked loop system of claim [[1]] **6**, further comprising a divider configured to divide the reference signal before passing it to the error detector.

38. (Original) The phase-locked loop system of claim 37, where the divider output is used as an enable for the reference signal input of the error detector.

39-44. (Canceled)

45. (Currently Amended) The method of claim [[44]] **48**, where the plurality of derivative signals are generated in regular fixed phase relationships with the primary output signal.

46. (Original) The method of claim 45, where the regular fixed phase relationships uniformly span 360 degrees.

47. (Original) The method of claim 46, where the regular fixed phase relationships are 0, -90, -180, -270 degrees.

48. (Currently Amended) **A phase-locked loop method, comprising:**

receiving a reference signal;

producing a primary output signal that tends toward a predefined frequency relationship with the reference signal;

generating a plurality of derivative signals based on the primary output signal; and

producing a feedback signal based on the plurality of derivative signals,

~~The method of claim 44,~~ where producing [[a]] **the** feedback signal based on the plurality of derivative signals includes multiplexing the plurality of derivative signals together to form the feedback signal.

49. (Original) The method of claim 48, where multiplexing the plurality of derivative signals includes selecting from among of a plurality of VCO output signals to form the feedback signal.

50. (Original) The method of claim 48, where multiplexing includes reading an incrementer output value produced by an incrementer, and selecting a derivative signal to include in the feedback signal based on the incrementer output value.

51. (Original) The method of claim 50, further comprising clocking the incrementer with the feedback signal.

52. (Original) The method of claim 50, further comprising producing the incrementer output value at least in part by summing incrementer input values over a period of time.

53. (Original) The method of claim 50, where reading an incrementer output value includes reading an integer component of the incrementer output value, and selecting a derivative signal includes selecting a multiplexer input based on the integer component of the incrementer output value.

54. (Original) The method of claim 50, wherein the incrementer output value is produced based on an incrementer input value with a fractional component.

55. (Original) The method of claim 54, where the step of producing the feedback signal further includes producing a feedback signal that does not have a constant cycle time, due to the fractional component of the incrementer input value.

56. (Original) The method of claim 55, further comprising generating a correcting pulse in response to a detected phase error between the reference signal and the feedback signal.

57. (Original) The method of claim 56, further comprising filtering the correcting pulse through a filter network, the filter network being configured to eliminate output ripple from the correcting charge pump.

58. (Original) The method of claim 57, further comprising generating a canceling pulse to compensate for the correcting pulse.

59. (Original) The method of claim 58, where the canceling pulse is opposite of the correcting pulse.

60. (Original) The method of claim 58, where generating the canceling pulse is accomplished at least in part by keeping the pulse width of the canceling pulse constant and varying the amplitude of the canceling pulse.

61. (Original) The method of claim 58, further comprising generating the canceling pulse based on current supplied by a current source that is controlled by a fractional component of the incrementer output value.

62. (Withdrawn) The method of claim 58, where the correcting pulse is generated by a correcting integrating charge pump and where the canceling pulse is generated by a correcting proportional charge pump, the method further comprising:

generating an integrating canceling pulse via an integrating canceling pump; and

generating a proportional canceling pulse via a proportional canceling pump.

63. (Withdrawn) The method of claim 62, where producing the feedback signal further includes generating a leading or trailing feedback signal that is routed to a canceling error detector coupled to the canceling charge pump.

64. (Currently Amended) The method of claim [[44]] **48**, further comprising dividing the feedback signal by a predetermined value.

65. (Currently Amended) The method of claim [[44]] **48**, further comprising dividing the reference signal by a predetermined value.

66-68. (Canceled)